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*Title:*

**DYNAMIC CIRCUITS USING EXCLUSIVE STATES**

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DYNAMIC CIRCUITS USING EXCLUSIVE STATES

FIELD OF THE INVENTION:

The invention relates to dynamic circuits.

5    BACKGROUND:

Dynamic circuits are not robust under noisy condition. For example, a typical dynamic domino circuit uses a half or full latch to hold its dynamic nodes. However, under noisy conditions, these nodes can couple to noise and lose their data. Thus, a need exists for a dynamic domino circuit that is robust under noisy condition.

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As another example, in many kinds of dynamic adders, inversion of carry that is required at the end of the carry chain is either accomplished by using a static inverter (extra gate delay) followed by static circuits, or having a separate chain of logic to generate carry bar (area penalty). For a really fast implementation, four chains of logic 15 ( $g, \sim g, p, \sim p$ ) are needed, thereby consuming a lot of area. Thus, a need exists for a dynamic adder that does not use a static inverter that causes extra gate delay. A further need exists for a dynamic adder that does not consume a lot of area.

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Furthermore, in most dynamic adders, a latch is required at the output to preserve 20 the generated sum during circuit precharge. A need exists to improve the speed of the adders by cutting the latch delay while not requiring complex clocking.

**SUMMARY:**

The invention provides a dynamic domino circuit that is robust under noisy condition. The invention provides a dynamic adder that does not use a static inverter that causes extra gate delay. The invention also provides a dynamic adder that does not  
5 consume a lot of area. The invention also improves speed of the adders by cutting the latch delay while not requiring complex clocking.

Preferably, a dynamic circuit includes a logic portion and three dynamic output portions, each of which having a dynamic node for holding data. A first and a second  
10 transistors have their gates coupled to the first dynamic node. The first transistor has its drain coupled to the second dynamic node, and the second transistor has its drain coupled to the third dynamic node. A third and a fourth transistors have their gates coupled to the second dynamic node. The third transistor has its drain coupled to the first dynamic node, and the fourth transistor has its drain coupled to the third dynamic node. A fifth  
15 and a sixth transistors having their gates coupled to the third dynamic node. The fifth transistor has its drain coupled to the first dynamic node, and the sixth transistor has its drain coupled to the second dynamic node.

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BRIEF DESCRIPTION OF THE FIGURES:

Figure 1 shows a dynamic domino circuit in accordance with one embodiment of the invention.

5       Figure 2 shows a dynamic adder in accordance with one embodiment of the invention.

Figure 3A shows a multiplexer implementing dynamic select inputs in accordance with one embodiment of the invention.

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Figure 3B shows a blow up view of the multiplexer from Figure 3A.

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DETAILED DESCRIPTION:

Reference is made in detail to the preferred embodiments of the invention. While the invention is described in conjunction with the preferred embodiments, the invention is not intended to be limited by these preferred embodiments. On the contrary, the

5 invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

Furthermore, in the following detailed description of the invention, numerous specific details are set forth in order to provide a thorough understanding of the invention.

However, as is obvious to one ordinarily skilled in the art, the invention may be practiced

10 without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so that aspects of the invention will not be obscured.

Referring now to Figure 1, a dynamic domino circuit 100 is shown in accordance  
15 with one embodiment of the invention. Circuit 100 comprises of a logic portion 110 coupled to three dynamic output portions 120, 130 and 140. Dynamic output portion 120 is used for holding data for the propagate signal (p). Dynamic output portion 130 is used for holding data for the generate signal (g). Dynamic output portion 140 is used for holding data for the kill signal (k).

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Referring still to Figure 1, dynamic output portion 120 comprises an inverter 121, transistors 122 and 123, and dynamic node 124. Dynamic output portion 130 comprises an inverter 131, transistors 132 and 133, and dynamic node 134. Dynamic output portion 140 comprises an inverter 141, transistors 142 and 143, and dynamic node 144.

Transistors 132 and 142 are coupled to dynamic node 124. Transistors 122 and 143 are coupled to dynamic node 134. Transistor 123 and 133 are coupled to dynamic node 144. Assume dynamic nodes 124, 134 and 144 are mutually exclusive. That is to say, one and only one dynamic node among nodes 124, 134 and 144 will be at logic zero when the

5      clock is high. As such, when dynamic node 124 holds a logic zero, dynamic node 134 holds a logic one and dynamic node 144 holds a logic one. Similarly, when dynamic node 134 holds a logic zero, dynamic node 124 holds a logic one and dynamic node 144 holds a logic one. Also similarly, when dynamic node 144 holds a logic zero, dynamic node 124 holds a logic one and dynamic node 134 holds a one.

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This exclusive property can be used to ensure that the dynamic nodes 124, 134 and 144 will recover fully from noise. Specifically, as an example, a logic zero being held on dynamic node 124 turns on transistor 132 to provide a current to ensure that a logic one is held in dynamic node 134. As such, if a noise spike occurs at dynamic node  
15      134 to change the logic one held therein into a logic zero, the current supplied by transistor 132 recovers the logic one at dynamic node 134. Also, a logic zero being held on dynamic node 124 turns on transistor 142 to provide a current to ensure that a logic one is held in dynamic node 144. As such, if a noise spike occurs at dynamic node 144 to change the logic one held therein into a logic zero, the current supplied by transistor  
20      142 recovers the logic one at dynamic node 144. As understood herein, the idea of noise recoverability applies not only to circuit 100, but to any class of dynamic circuit that uses exclusive signals.

Continuing with Figure 1, the same theory holds when node 134 is being held at logic zero and nodes 124 and 134 are being held at logic one. The same theory also holds when node 144 is being held at logic zero and nodes 124 and 134 are being held at logic one.

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Referring now to Figure 2, a portion of a carry chain 205 of a dynamic adder 200 is shown in accordance with one embodiment of the invention. Each of dynamic circuits 211-217 is used to generate successive levels of propagate (p), generate (g), and kill (k) signals. Each set of p, g, and k at each level is mutually exclusive. True dynamic inversion at any point in carry chain 205 can be achieved as a simple function of true terms.

10 As an example, referring still to Figure 2, consider nodes k0, g0, and p0 as shown. Inversion of each of these nodes can be implemented in the form of the following simple equations:

$$\sim p_0 = g_0 + k_0,$$

$$\sim g_0 = p_0 + k_0, \text{ and}$$

$$\sim k_0 = g_0 + p_0.$$

Similar equations apply for inversion at all other levels of carry chain 205.

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20 By using true terms to generate complements, a common problem in dynamic signal inversion is circumvented. In a regular dynamic circuit, inversion is frequently implemented by demorganization all the way to the beginning of carry chain 205. In so doing, four terms (generate (g), generate bar ( $\sim g$ ), propagate (p), and propagate bar ( $\sim p$ ))

are required per dynamic circuit. On the other hand, by using only three terms rather than the conventional four terms, more area can be saved.

- Referring now to Figure 3A, a final stage of a dynamic adder 300 is shown in
- 5 accordance with one embodiment of the invention. A sum stage mux circuit 340 is coupled to a dynamic logic 310 and a dynamic carry chain 320. A latch 350 is built into mux circuit 340 such that no additional delay is introduced in the critical path of adder 300. Controlling inputs sel 331 and ~sel 332 are used both as selection signals for mux circuit 340 and also as a clock for latch 350.

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- Referring now to Figure 3B, a detailed diagram of mux circuit 340 is shown in accordance with one embodiment of the invention. As shown, mux circuit 340 includes latch 350 coupled to input d0 361, input d1 362, sel 331 and ~sel 332. When the clock is high, dynamic nodes sel 331 and ~sel 332 evaluate to their respective logic, thereby 15 functioning as select inputs to mux circuit 340. When the clock is low, sel 331 and ~sel 332 precharge to logic zero, thereby cutting off transmission gates 371 and 372. In turn, latch 350 will hold the state of mux circuit 340 for the remainder of the clock cycle. As such, a latch has been implemented with neither additional delay nor any complex clocking.

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